PORTAL
US Patent & Trademark Office

Subscribe (Full Service) Register (Limited Service, Free) Login

Search: ● The ACM Digital Library ○ The Guide

Bug list <and> input vector

THE ACM DIGITAL LIBRARY

Feedback Report a problem Satisfaction survey

Terms used **Bug list** and **input vector**

Found **101,935** of **150,885**

Sort results by: relevance

Display results: expanded form

Save results to a Binder

Search Tips

☐ Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

Best 200 shown

Relevance scale

1 A program testing assistant
David Chapman
September 1982 **Communications of the ACM**, Volume 25 Issue 9
Full text available: pdf(1.08 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes the design and implementation of a program testing assistant which aids a programmer in the definition, execution, and modification of test cases during incremental program development. The testing assistant helps in the interactive definition of test cases and executes them automatically when appropriate. It modifies test cases to preserve their usefulness when the program they test undergoes certain types of design changes. The testing assistant acts ...

2 Enhancing simulation with BDDs and ATPG
Malay K. Ganai, Adnan Aziz, Andreas Kuehlmann
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(795.60 KB) Additional Information: full citation, references, citings, index terms

Keywords: ATPG, BDDs, coverage, formal verification, simulation

3 Scalable error detection using boolean satisfiability
Yichen Xie, Alex Aiken
January 2005 **Proceedings of the 32nd ACM SIGPLAN-SIGACT sysposium on Principles of programming languages**
Full text available: pdf(276.56 KB) Additional Information: full citation, abstract, references, index terms

We describe a software error-detection tool that exploits recent advances in boolean satisfiability (SAT) solvers. Our analysis is path sensitive, precise down to the bit level, and models pointers and heap data. Our approach is also highly scalable, which we achieve using two techniques. First, for each program function, several optimizations compress the size of the boolean formulas that model the control- and data-flow and the heap locations accessed by a function. Second, summaries in the sp ...

Keywords: boolean satisfiability, error detection, program analysis

4 Software reliability via run-time result-checking
Hal Wasserman, Manuel Blum
November 1997 **Journal of the ACM (JACM)**, Volume 44 Issue 6

Full text available: pdf(150.60 KB) Additional Information: full citation, abstract, references, citings, index terms, review

We review the field of result-checking, discussing simple checkers and self-correctors. We argue that such checkers could profitably be incorporated in software as an aid to efficient debugging and enhanced reliability. We consider how to modify traditional checking methodologies to make them more appropriate for use in real-time, real-number computer systems. In particular, we suggest that checkers should be allowed to use stored randomness: that is, that they should be allowed to generate ...

Keywords: Fourier transform, built-in testing, concurrent error detection, debugging, fault tolerance, result-checking, self-correcting

5 Bug isolation via remote program sampling
Ben Liblit, Alex Aiken, Alice X. Zheng, Michael I. Jordan
May 2003 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 2003 conference on Programming language design and implementation**, Volume 38 Issue 5
Full text available: pdf(258.37 KB) Additional Information: full citation, abstract, references, index terms

We propose a low-overhead sampling infrastructure for gathering information from the executions experienced by a program's user community. Several example applications illustrate ways to use sampled instrumentation to isolate bugs. Assertion-dense code can be transformed to share the cost of assertions among many users. Lacking assertions, broad guesses can be made about predicates that predict program errors and a process of elimination used to whittle these down to the true bug. Finally, even ...

Keywords: assertions, bug isolation, feature selection, logistic regression, random sampling, statistical debugging

6 Technical papers: dynamic program analysis: Tracking down software bugs using automatic anomaly detection
Sudheendra Hangal, Monica S. Lam
May 2002 **Proceedings of the 24th International Conference on Software Engineering**
Full text available: pdf(1.30 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper introduces DIDUCE, a practical and effective tool that aids programmers in detecting complex program errors and identifying their root causes. By instrumenting a program and observing its behavior as it runs, DIDUCE dynamically formulates hypotheses of invariants obeyed by the program. DIDUCE hypothesizes the strictest invariants at the beginning, and gradually relaxes the hypothesis as violations are detected to allow for new behavior. The violations reported help users to catch soft ...

7 New tools and methods for future embedded SoC: Debugging HW/SW interface for MPSoC: video encoder system design case study
Mohamed-Wassim Youssef, Sungjoo Yoo, Arif Sasongko, Yanick Paviot, Ahmed A. Jerraya
June 2004 **Proceedings of the 41st annual conference on Design automation**
Full text available: pdf(277.58 KB) Additional Information: full citation, abstract, references, index terms

This paper reports a case study of multiprocessor SoC (MPSoC) design of a complex video encoder, namely OpenDivX. OpenDivX is a popular version of MPEG4. It requires massive computation resources and deals with complex data structures to represent video streams. In this study, the initial specification is given in sequential C code that had to be parallelized to be executed on four different processors. High level programming model, namely Message Passing Interface (MPI) was used to enable inter ...

Keywords: debug, hardware-dependant software, hardware-software interface, multiprocessor system-on-chip

8 BUGSYS: a programming system for picture processing—not for debugging
R. S. Ledley, J. Jacobsen, M. Belson
February 1966 **Communications of the ACM**, Volume 9 Issue 2
Full text available: pdf(1.39 MB) Additional Information: full citation, abstract, references, citings

BUGSYS is a picture processing and measuring system that depends upon a pictorial input to the computer's memory. BUGSYS can be used for many types of applications. In particular, the authors have used the system for the analysis of linear graphs. The main concept of the system is the use of a collection of programmable pointers, which are visualized as a family of "bugs."

9 Automatic lighthouse generation for directed state space search
Praveen Yalagandula, Vigyan Singhal, Adnan Aziz
January 2000 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(94.43 KB) Publisher Site Additional Information: full citation, references, citings, index terms

10 Performance issues and error analysis in an open-domain question answering system
Dan Moldovan, Marius Paşca, Sanda Harabagiu, Mihai Surdeanu
April 2003 **ACM Transactions on Information Systems (TOIS)**, Volume 21 Issue 2
Full text available: pdf(270.12 KB) Additional Information: full citation, abstract, references, index terms

This paper presents an in-depth analysis of a state-of-the-art Question Answering system. Several scenarios are examined: (1) the performance of each module in a serial baseline system, (2) the impact of feedbacks and the insertion of a logic prover, and (3) the impact of various retrieval strategies and lexical resources. The main conclusion is that the overall performance depends on the depth of natural language processing resources and the tools used for answer finding.

Keywords: Question answering, natural language applications, performance analysis, text retrieval

11 Project notes and demos: Processing self corrections in a speech to speech system
Jörg Spilker, Martin Klarner, Günther Görz
July 2000 **Proceedings of the 17th conference on Computational linguistics - Volume 2**
Full text available: pdf(462.70 KB) Additional Information: full citation, abstract, references

Speech repairs occur often in spontaneous spoken dialogues. The ability to detect and correct those repairs is necessary for any spoken language system. We present a framework to detect and correct speech repairs where all relevant levels of information, i. e., acoustics, lexis, syntax and semantics can be integrated. The basic idea is to reduce the search space for repairs as soon as possible by cascading filters that involve more and more features. At first an acoustic module generates hypothe ...

12 A Heuristic to Determine Low Leakage Sleep State Vectors for CMOS Combinational Circuits
Rahul M. Rao, Frank Liu, Jeffrey L. Burns, Richard B. Brown
November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(126.92 KB) Additional Information: full citation, abstract, index terms

Input vector control has been used to minimize the leakage powerconsumption of a circuit in sleep state. In this paper, we presenta novel heuristic for determining a low leakage vector to beapplied to a circuit in sleep state. The heuristic is a greedy searchbased on the controllability of nodes in the circuit and uses thefunctional dependencies among cells in the circuit to guide thesearch. Results on a set of ISCAS and MCNC benchmark circuitsshow that in all cases our heuristic returns a vecto ...

13 Multiple viewpoint rendering
Michael Halle
July 1998 **Proceedings of the 25th annual conference on Computer graphics and interactive techniques**
Full text available: pdf(3.89 MB) Additional Information: full citation, references, citings, index terms

14 Leakage power optimization: Implicit pseudo boolean enumeration algorithms for input vector control
Kaviraj Chopra, Sarma B. K. Vrudhula
June 2004 **Proceedings of the 41st annual conference on Design automation**
Full text available: pdf(159.13 KB) Additional Information: full citation, abstract, references, index terms

In a CMOS combinational logic circuit, the subthreshold leakage current in the standby state depends on the state of the inputs. In this paper we present a new approach to identify the minimum leakage set of input vectors (MLS). Applying a vector in the MLS is known as Input Vector Control (IVC), and has proven to be very useful in reducing gate oxide leakage and sub-threshold leakage in standby mode of operation. The approach presented here is based on *Implicit Enumeration* of integer-val ...

Keywords: CMOS, SAT, binary decision diagrams, leakage, power, symbolic methods

15 Conscientious programming using PMA
Guy Barker, Douglas J. Keenan, Herman van Loon
May 1990 **ACM SIGAPL APL Quote Quad , Conference proceedings on APL 90: for the future**, Volume 20 Issue 4
Full text available: pdf(773.06 KB) Additional Information: full citation, abstract, references, citings, index terms, review

This paper describes the use of APL systems at Philips to assist in providing a controlled application support environment and examines in detail an APL software management system, PMA (Program Maintenance Aid).

16 Term-list translation using mono-lingual word co-occurrence vectors
Genichiro Kikui
August 1998
Full text available: pdf(467.21 KB) Publisher Site Additional Information: full citation, abstract, references

A term-list is a list of content words that characterize a consistent text or a concept. This paper presents a new method for translating a term-list by using a corpus in the target language. The method first retrieves alternative translations for each input word from a bilingual dictionary. It then determines the most 'coherent' combination of alternative translations, where the coherence of a set of words is defined as the proximity among multi-dimensional vectors produced from the words on th ...

17 Querying web metadata: Native score management and text support in databases
Gültekin Özsoyo□lu, Ismail Sengör Altingövde, Abdullah Al-Hamdani, Selma Ayşe Özel, Özgür Ulusoy, Zehra Meral özsoyo□lu
January 2004 **ACM Transactions on Database Systems (TODS)**, Volume 29 Issue 4
Full text available: pdf(737.76 KB) Additional Information: full citation, abstract, references, index terms

In this article, we discuss the issues involved in adding a native score management system to object-relational databases, to be used in querying Web metadata (that describes the semantic content of Web resources). The Web metadata model is based on topics (representing entities), relationships among topics (called *metalinks*), and importance scores (sideway values) of topics and metalinks. We extend database relations with scoring functions and importance scores. We add to SQL score-manag ...

Keywords: Score management for Web applications

18 A C-based RTL design verification methodology for complex microprocessor
Joon-Seo Yim, Yoon-Ho Hwang, Chang-Jae Park, Hoon Choi, Woo-Seung Yang, Hun-Seung Oh, In-Cheol Park, Chong-Min Kyung
June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**
Full text available: pdf(224.80 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

As the complexity of high-performance microprocessor increases,functional verification becomes more and more difficultand RTL simulation emerges as the bottleneck of thedesign cycle.In this paper, we suggest C language-based designand verification methodology to enhance the simulationspeed instead of the conventional HDL-based methodologies.RTL C model (StreC) describes the cycle-based behaviors ofsynchronous circuits and is followed by model refining andoptimization using LifeTime Analyzer (LTA ...

19 Special session on on-chip multi-processing: Design experience of a chip multiprocessor merlot and expectation to functional verification
Satoshi Matsushita
October 2002 **Proceedings of the 15th international symposium on System Synthesis**
Full text available: pdf(797.44 KB) Additional Information: full citation, abstract, references, index terms

We have fabricated a Chip Multiprocessor prototype code-named Merlot to proof our novel speculative multithreading architecture. On Merlot, multiple threads provide wider issue window beyond ordinal instruction level parallel (ILP) processors like superscalar or VLIW. With the architecture, we estimate 3.0 times speedup against single processing elements (PE) on speech recognition code and IDCT code with four PEs. Merlot integrates on-chip devices, PCI interface, and SDRAM interfaces. We have en ...

Keywords: CMP, chip multiprocessor, deign experience, functional verification, speculative multithreading

20 Practical approaches to the verification of a telecom megacell using FormalCheck
Leila Barakatain, Sofiène Tahar, Jean Lamarche, Jean-Marc Gendreau
March 2001 **Proceedings of the 11th Great Lakes symposium on VLSI**
Full text available: pdf(58.06 KB) Additional Information: full citation, references, index terms

Results 1 - 20 of 200   Result page: **1** 2 3 4 5 6 7 8 9 10 next